AMENDMENTS TO THE CLAIMS

Please amend claim 1 as follows.

Claim 1 (currently amended) A circuit for interleaving a data stream, comprising:

a buffer storage circuit having an input coupled for receiving and storing the data stream;

a first memory circuit having an input coupled to an output of the buffer storage circuit for receiving a first section of the data stream;

a second memory circuit having an input coupled to the output of the buffer storage circuit for receiving a second section of the data stream wherein the first and second sections of the data stream are representative of different channels of an audio signal, wherein the first memory circuit stores less than an entire frame of audio data and wherein the second memory circuit stores less than the entire frame of audio data; and

a multiplexer circuit having first and second inputs respectively coupled to the outputs of the first and second memory circuits for selecting between the first and second sections in response to a selection signal to provide an interleaved output signal at an output.

Claim 2 (cancelled)

Claim 3 (original) The circuit of claim 1, wherein the first and second sections of the data stream are formatted as an audio portion of Motion Picture Experts Group 2 (MPEG-2) data.

Claim 4 (original) The circuit of claim 1, wherein the first memory circuit includes a dual port memory for providing stored data at the output of the first memory circuit while receiving and storing other data from the buffer storage circuit.

Claim 5 (original) The circuit of claim 4, wherein the second memory circuit includes a dual port memory for providing stored data at the output of the second memory circuit while receiving and storing new data from the buffer storage circuit.

Claim 6 (original) The circuit of claim 1, wherein the first memory circuit has a control input responsive to a first control signal for receiving first data from the buffer storage circuit after an amount of data stored in tile first memory circuit falls below a predetermined value.

Claim 7 (original) The circuit of claim 6, wherein the second memory circuit has a control input responsive to a second control signal for receiving second data from the buffer storage circuit after an amount of data stored in the first memory circuit falls below a predetermined value.

Claim 8 (original) The circuit of claim 7, further including a memory control circuit having first and second outputs coupled to control inputs of the first and second memory circuits for providing the first and second control signals, respectively.

Claim 9-14 (cancelled)

Claim 15 (previously presented) A method of interleaving a data stream, comprising the steps of:

storing the data stream including storing data of the first section of the data stream and data of the second section of the data stream in a third memory location;

copying a first section of file data stream to a first memory location;

copying a second section of the data stream to a second memory location;

selecting between the first and second memory locations to produce an interleaved output signal and selecting between data stored in the first memory location and data stored in the second memory location, wherein the step of selecting includes:

transferring data from the third memory location to the first memory location in response to a first control signal; and

incrementing a first pointer representative of an amount of data stored in the first memory location;

decrementing the first pointer as data stored in the first memory location is selected; and

generating the first control signal after the first pointer decrements to a first predetermined value.

Claim 16 (original) The method of claim 15, wherein the step of selecting the second data includes the steps of:

transferring data from the third memory location to the second memory location in response to a second control signal; and

incrementing a second pointer representative of an amount of data stored in the second memory location.

Claim 17 (original) The method of claim 16, wherein the step of selecting the second data further includes the steps of:

decrementing the second pointer as data stored in the second memory location is selected; and

generating the second control signal after the second pointer decrements to a second predetermined value.

Claim 18-20 (cancelled)